**Design the memory map and memory decoder for a 16 bits microprocessor (20 address lines) system using the following memory requirements:**

**- 128KB ROM, using 64K x 16 bits memories**

**- 256KB SRAM, using 128K x 16 bits memories, at the beginning**

**- 512KB DRAM, using 128K x 16 bits memories**

**STEP 1**

**STEP 2**

**STEP 3**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ***BLOCK*** | ***BLOCK SIZE*** | ***ADDRESS LINES*** | ***ADDRESS RANGE*** | | ***BLOCK SIZE (hexa)*** |
| B1 | 128 KB | 17 | 0x0\_0000 | 0x1\_FFFF | 0x2\_0000 |
| B2 | 256 KB | 18 | 0x0\_0000 | 0x3\_FFFF | 0x4\_0000 |
| B3 | 256 KB | 18 | 0x0\_0000 | 0x3\_FFFF | 0x4\_0000 |
| B4 | 256 KB | 18 | 0x0000 | 0x3\_FFFF | 0x4\_0000 |

**STEP 4**

|  |  |  |
| --- | --- | --- |
| ***TYPE*** | ***BLOCK*** | ***MEMORY MAP*** |
| SRAM | B2 | 0x0\_0000 |
| 0x3\_FFFF |
| ROM | B1 | 0x4\_0000 |
| 0x5\_FFFF |
| DRAM | B3 | 0x6\_0000 |
| 0x9\_FFFF |
| B4 | 0xA\_0000 |
| 0xD\_FFFF |